COMPLETE LISTING OF CLAIMS

IN ASCENDING ORDER WITH STATUS INDICATOR

Claims 1-74. (Cancelled)

75. (New) A semiconductor structure comprising:

at least one isolation region formed within a semiconductor substrate; and

a plurality of gate stacks over said semiconductor substrate, at least two of said plurality of gate stacks being in contact with said isolation region and being spaced apart from each other by about 100 Angstroms to about 400 Angstroms.

76. (New) The semiconductor structure of claim 75, wherein said plurality of gate stacks is spaced apart from each other by about 100 Angstroms to about 300 Angstroms.

77. (New) The semiconductor structure of claim 75, wherein said plurality of gate stacks further comprises a plurality of gate layers over said substrate and said isolation region.

78. (New) A memory structure comprising:

a plurality of word lines formed over a semiconductor substrate, at least two adjacent ones of said plurality of word lines being spaced apart from each other by a distance of about 100 to about 300 Angstroms.

79. (New) The memory structure of claim 78 further comprising a plurality of bit lines formed over and in contact with said plurality of word lines.

80. (New) The memory structure of claim 78 further comprising an isolation region formed below said at least two adjacent ones of said plurality of word lines being spaced apart from each other.

81. (New) The memory structure of claim 78, wherein each of said plurality of word lines further comprises a plurality of gate layers.

82. (New) The memory structure of claim 81, wherein each of said plurality of word lines includes a polysilicon layer.

83. (New) The memory structure of claim 81, wherein each of said plurality of word lines includes a metal silicide layer.

84. (New) The memory structure of claim 78, wherein said memory structure is a DRAM structure.

85. (New) The memory structure of claim 78, wherein said memory structure is a SRAM structure.

86. (New) A memory device comprising a plurality of DRAM cells, said DRAM cells including a plurality of word lines formed over a semiconductor substrate, at least two of said plurality of word lines being spaced apart from each other by a distance of about 100 to about 300 Angstroms, and a plurality of bit lines formed over said plurality of word lines.

87. (New) The memory device of claim 86 further comprising an isolation region formed below and in contact with said at least two of said plurality of word lines being spaced apart from each other.